What is claimed is:

1. A device for prolonging lifetime of nonvolatile memory, the device being connected with an electronic machine and a nonvolatile memory unit, comprising a RAM (Random Access Memory) buffer zone, a counter, and two sets of inverters, wherein:

the RAM buffer zone connected with the counter and the inverters is employed for temporary storage of a unit data train and a correspondent state flag during accessing when a host electronic machine is to read/write from or to a nonvolatile memory unit, wherein the state flag will indicate the operation state when the unit data train passes through the inverters;

the counter connected with the host electronic machine and the RAM buffer zone is in charge of counting the total bits of logic "0" in the unit data train and judging whether the counted result outnumbers a default proportion or not; if positive, the state flag corresponding to the unit data train is turned into "0", otherwise, into "1"; and

the interpolated inverters are arranged to check the corresponding state flag of the unit data train for inverse or non-inverse operation of the unit data train;

whereby the electronic machine will write lesser bits of logic "0" to prolong the lifetime of the nonvolatile memory unit.

2. The device according to claim 1, wherein each inverter comprises a non-inverse and an inverse inverter; and one of them is arranged en route of writing a unit data train to the nonvolatile memory unit while the other en route of reading a unit data train from the nonvolatile memory unit.